

ANALOG/DIGITAL CIRCUIT DESIGN IN SiGe FOR SPACE APPLICATIONS

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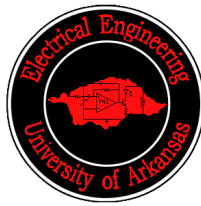
International Planetary Probe Workshop, JUNE 29, 2006

Outline

- 1. Variable Gain Amplifier Design**
- 2. Pipelined Circuit and Microcontroller Design**
- 3. Conclusion**



SiGe Integrated Electronics for Extreme Environments

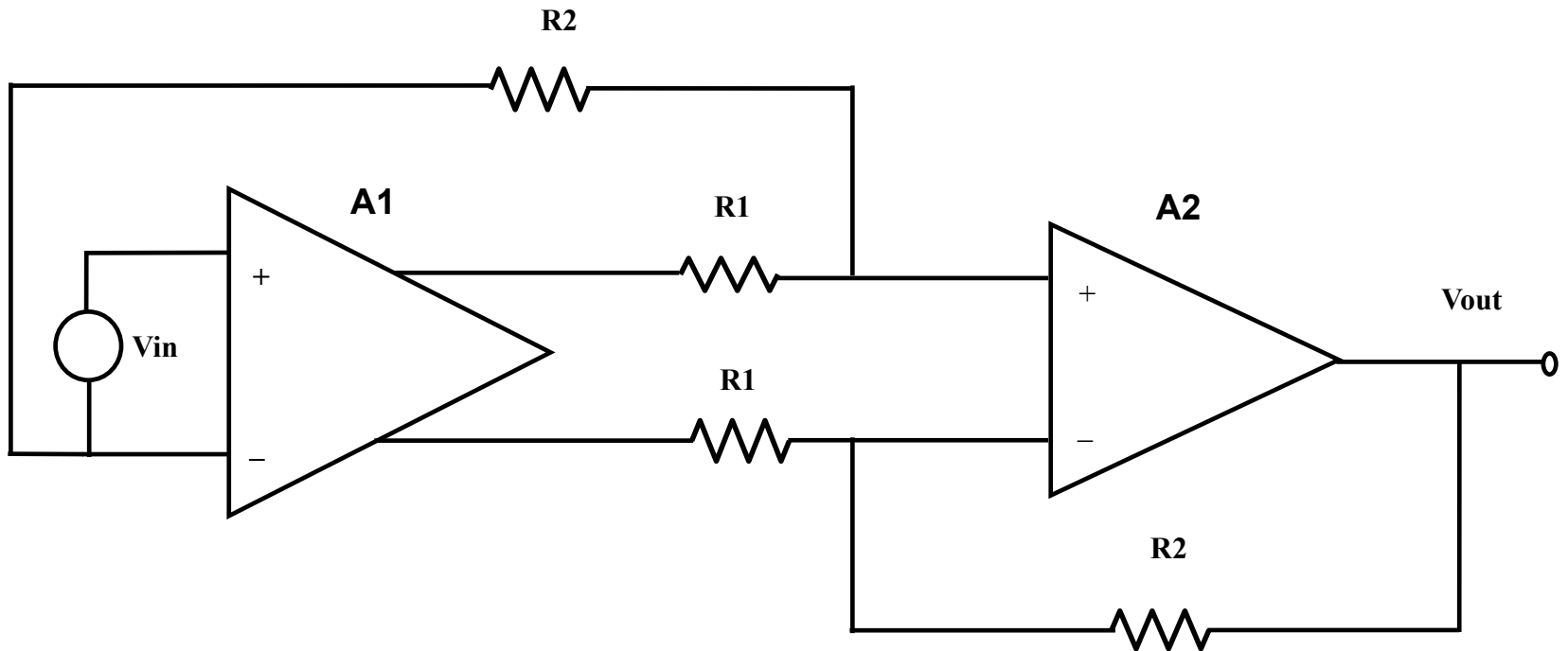


Challenge for Low Temperatures

Mixed-signal circuit design for low temperature environments is a challenge for several reasons:

- Transistor characteristics change significantly with temperature
- Difficult to match a large number of passive devices over a wide range of temperatures
- Standard reference circuits generally don't operate well over a large temperature range

VGA Circuit Design



$$A = \frac{R_L}{R_e} \frac{I_{ctrl}}{I_1} \frac{R_2}{R_1}$$

The diagram illustrates a two-stage CMOS operational amplifier. The first stage is a differential pair consisting of transistors Q1 and Q2, biased by a Wilson current mirror load (Q3, Q4, Q5, Q6, Q7, Q8) and a tail resistor. The second stage is a common-source amplifier (Q9, Q10) with a load capacitor C and resistors RL. The output is taken from the node between Q10 and the load. The circuit is biased by Ibias and Ictrl. The voltage gain is given by $A_1 = \frac{R_L}{R_e} \frac{I_{ctrl}}{I_1}$.

$$A_1 = \frac{R_L}{R_e} \frac{I_{ctrl}}{I_1}$$

For the first stage, Q3, Q4, Q5 and Q6 act as a feedback circuit for the differential pair Q1 and Q2. Transistor pairs Q3, Q5 and Q4, Q6 form CC-CE configurations.

$$\beta = g_m \frac{R_E}{2} = \frac{I_1}{V_T} \frac{R_E}{2}$$

$$A_{V1} \cong \frac{1}{\beta} = \frac{2V_T}{I_1 \cdot R_E}$$

$$A_{V2} = -\frac{I_{CTRL}}{2V_T} R_L$$

$$A_1 = A_{V1} A_{V2} = \frac{2V_T}{I_1 \cdot R_E} \frac{I_{CTRL}}{2V_T} \cdot R_L = \frac{I_{CTRL}}{I_1} \frac{R_L}{R_E}$$

Inversion Coefficient

$$IC = \frac{I_d}{I_S} = \frac{I_d}{2\mu_n C_{ox} U_T^2 (W/L)}$$

$IC < 0.1$ (Weak Inversion)

$0.1 < IC < 10$ (Moderate Inversion)

$IC > 10$ (Strong Inversion)

In strong inversion

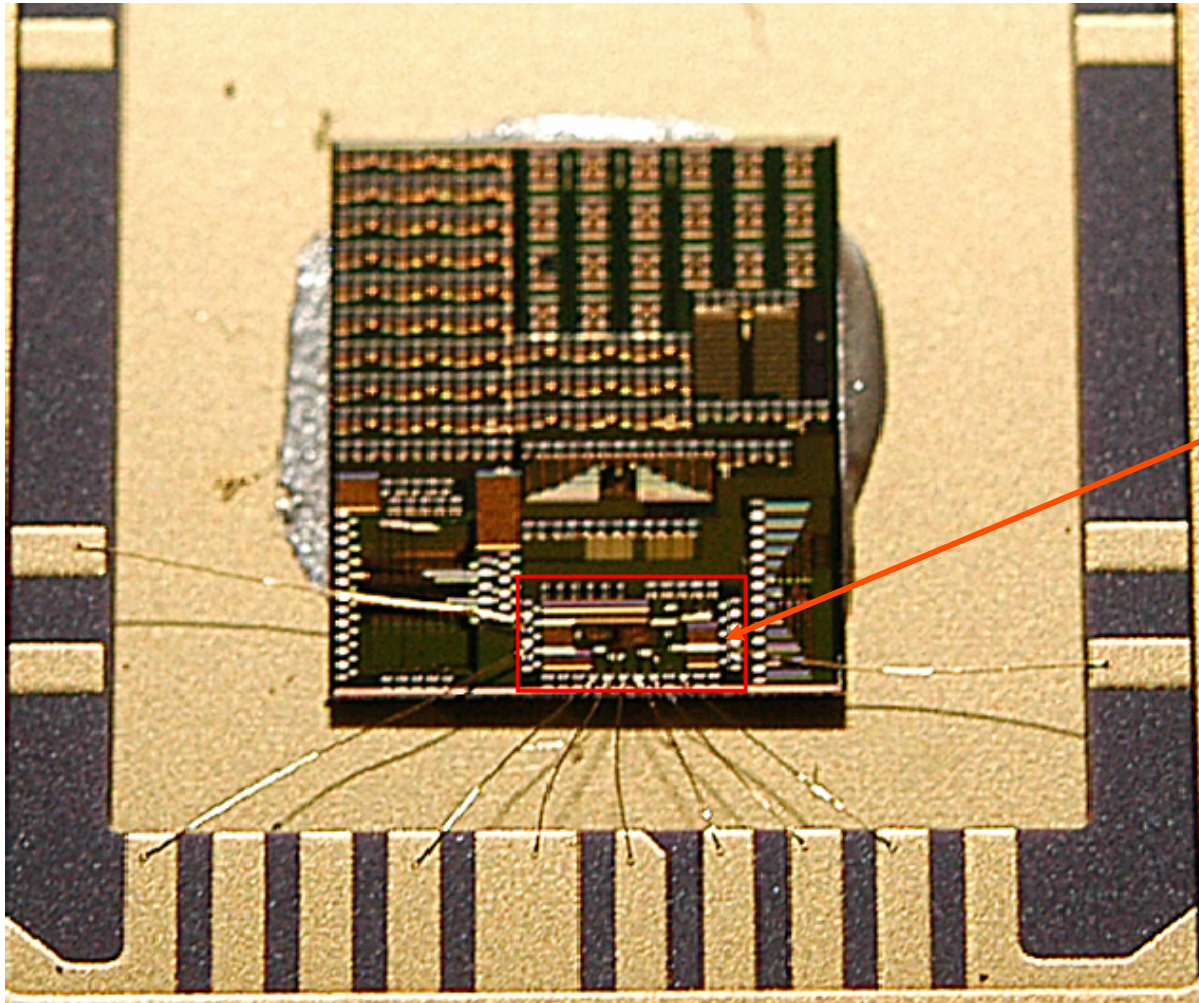
$$A_{V2} = \sqrt{\frac{kI_{S10}}{I_{D10}}} \frac{1}{2U_T} \left[\sqrt{\frac{kI_{S1}}{U_T^2} \frac{I_{D1}}{I_{D8}^2}} + \sqrt{\frac{kI_{S3}}{U_T^2} \frac{I_{D3}}{I_{D8}^2}} \right] V_A^2$$

Constant Inversion Coefficient

$$= \frac{1}{2} \left(\frac{kV_A}{U_T} \right)^2 \sqrt{\frac{1}{k} \frac{1}{IC_{10}}} \left[\sqrt{\frac{1}{k} \frac{1}{\eta_1} \frac{1}{IC_1}} + \sqrt{\frac{1}{k} \frac{1}{\eta_3} \frac{1}{IC_3}} \right]$$

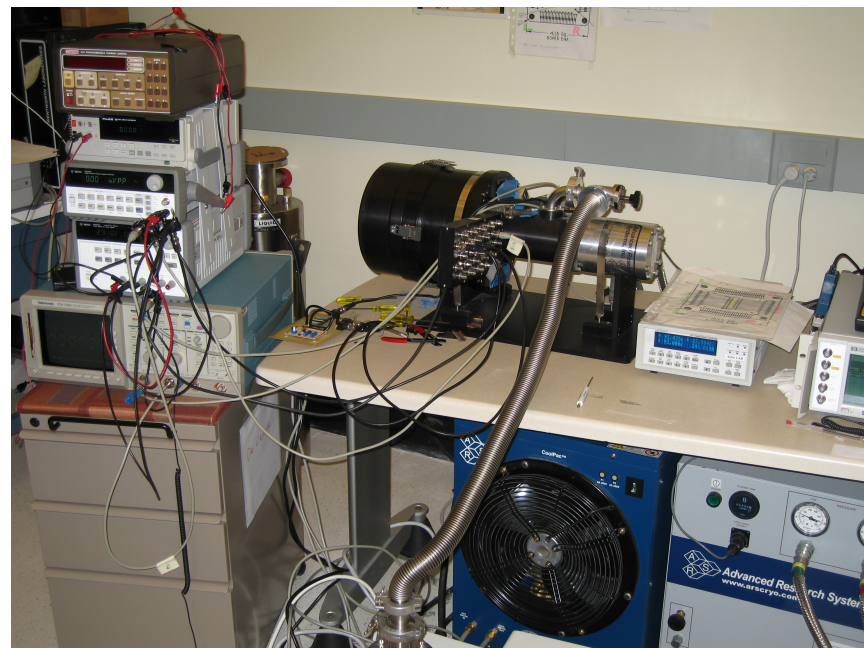
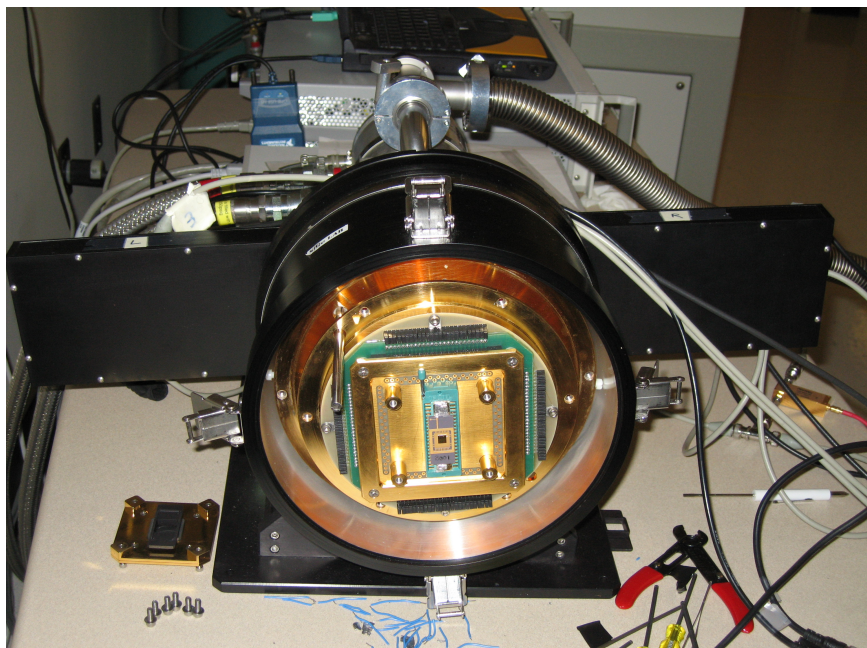
where $\eta_1 = \left(\frac{I_{D8}}{I_{D1}} \right)^2$ $\eta_3 = \left(\frac{I_{D8}}{I_{D3}} \right)^2$

Chip Photo

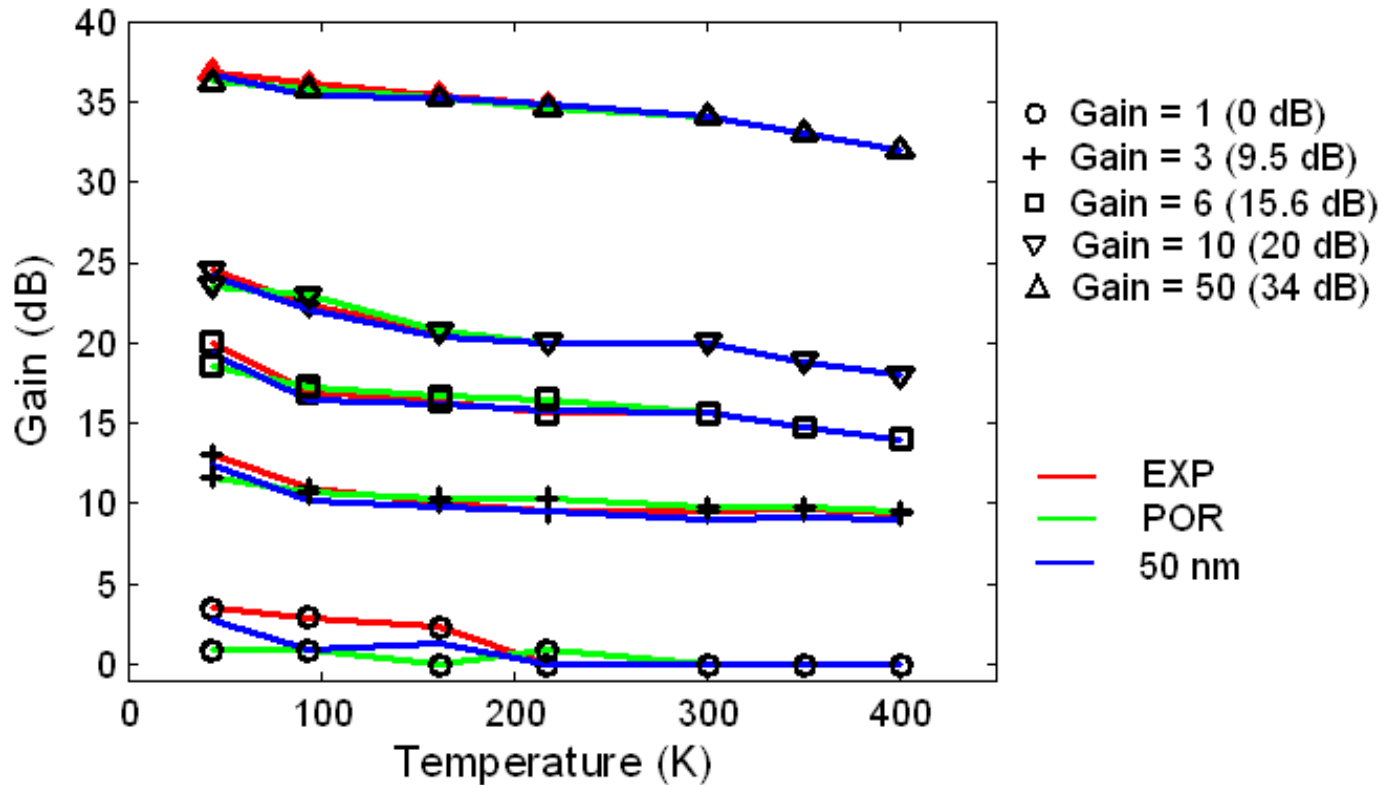


VGA

Package Cryo-Temperature Testing



Measurement Results



VGA works from - 230 °C to 125 °C !

Digital Circuits

At low temperature it is possible to reduce supply voltage to save power while maintaining the same performance

- The range of supply voltage scaling for synchronous circuits is limited (clock timing, worst case delay, etc.)
- Asynchronous circuits are more adaptable to changes in temperature and supply voltage
- A supply voltage scalability comparison of a synchronous digital circuit and two asynchronous counterparts under low temperature conditions is being researched
- Additionally, an Asynchronous Microcontroller is being designed that will work at cryogenic temperatures.

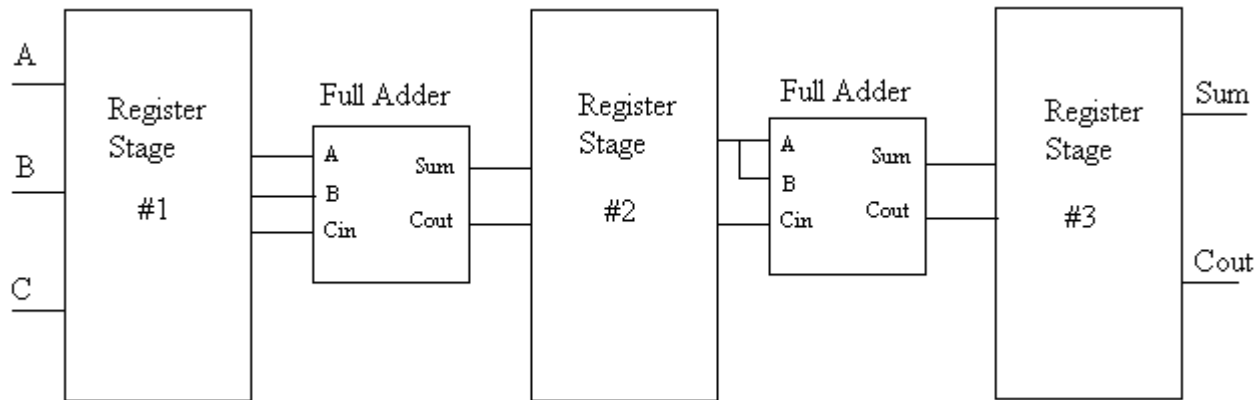
Asynchronous Design Methodologies

There are two different asynchronous logic design styles, namely, delay-insensitive and bounded-delay.

- The designed bounded-delay circuit used the traditional micropipeline structure approach. In this methodology, standard Boolean based combinational logic is combined with asynchronous control which employs C-elements.
- The delay-insensitive circuit design used NULL Convention LogicTM (NCL) which was developed by Theseus Logic, Inc. This type of asynchronous design employs dual-rail encoding to represent data and NULL states in order to incorporate control information to data and provide hysteresis.

Pipelined Circuit Design for Scalability Comparison

In order to make the comparison as fair as possible, the same circuit topology was constructed with all three design methods.



Topology for comparison circuits

Simulated Lowest Operating Voltages

The device models for simulating the $10\mu\times 1\mu$ MOS devices were available at single temperature points of -111°C , -180°C , and -230°C in addition to the standard IBM model that works for any temperature between 125°C and -55°C .

Simulated lowest operating voltages

Circuit Type	Temperature			
	25°C	-111°C	-180°C	-230°C
Synchronous Circuit	1.35 V	1.35 V	1.28 V	1.31 V
NCL Circuit	1.05 V	1 V	0.95 V	1 V
Bounded Delay Circuit	1.5 V	1.1 V	1.1 V	1.08 V

Asynchronous Microcontroller Core

- A simple microcontroller core has been designed using the delay-insensitive NULL Convention Logic (NCL) paradigm.
- NCL is a self timed logic design in which control is inherent , so there is no need for worse-case delay analysis and control path delay matching .
- Currently this microcontroller is being simulated for supply voltage scalability using the same low temperature models. It is also being laid out and will be ready for fabrication and testing.

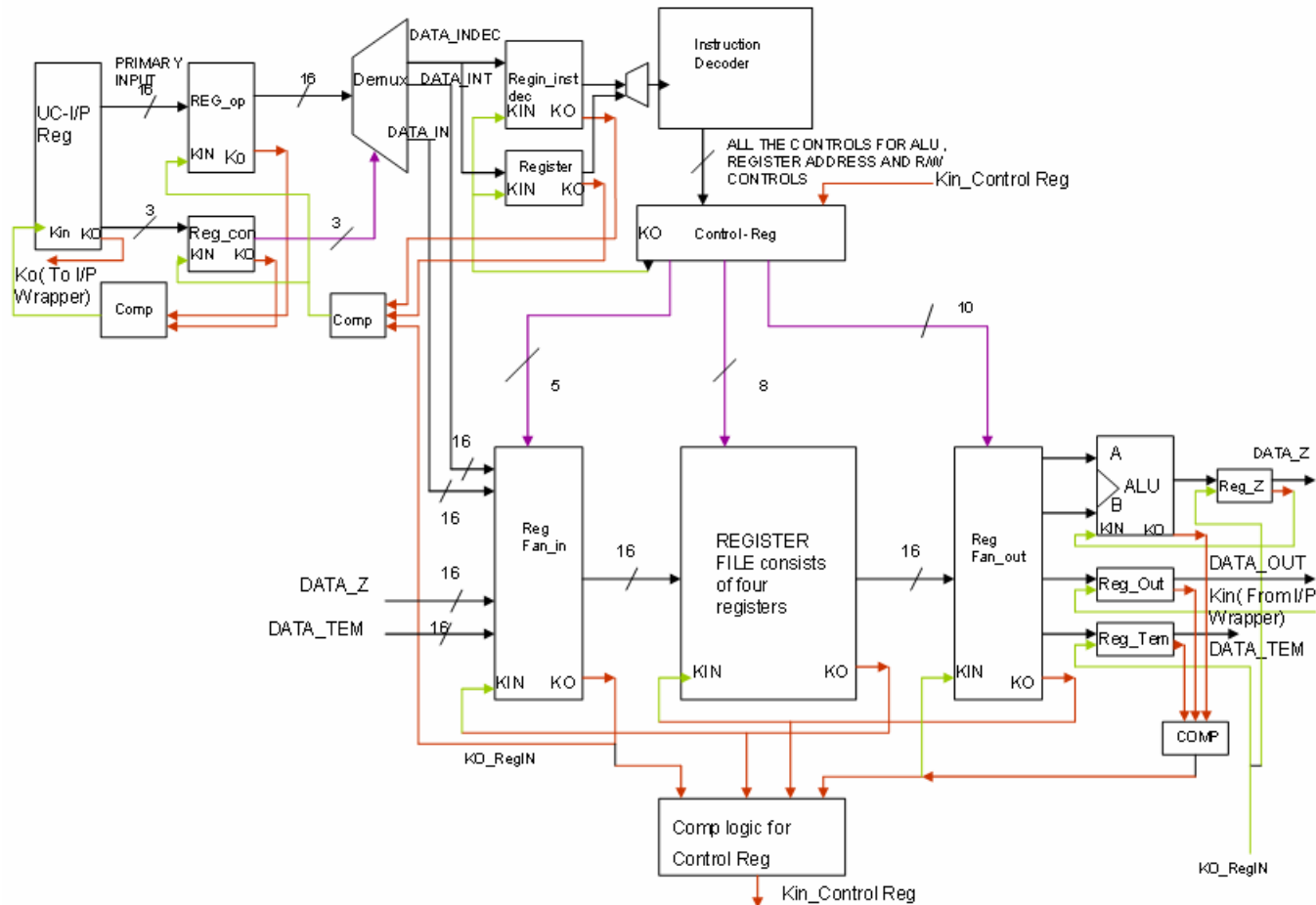
Features

- The processor mainly consists of Instruction Decoder (I), Register File (R) and Arithmetic Logic Unit (ALU).
- There are two interfacing circuits (wrappers) at the input and output to communicate with any synchronous devices.
- It has one external interrupt signal

Instruction Set

Operation Type	Instruction Type	Mnemonics	Description
Data Transfer	LOAD	LD Rx	This instruction is followed by the data which is stored in the Rx register.
	MOVE	MOV Rx, Ry	The contents of Ry is moved to Rx
	OUT	OUT Rx	The contents of Rx are read from microcontroller
Logical	AND	AND Rx ,Ry	The operands of Rx and Ry are ANDed and result is stored in Rx.
	OR	OR Rx ,Ry	The operands of Rx and Ry are ORed and result is stored in Rx
	XOR	XOR Rx ,Ry	The operands of Rx and Ry are XORed and result is stored in Rx
Arithmetic	ADD	ADD Rx ,Ry	The operands of Rx and Ry are ADDED and result is stored in Rx
	NOT	NOT Rx	The operands of Rx are complemented.

Top-Level Design of the Microcontroller Core



Components of the Microcontroller Core

Instruction Decoder

- It's a combinational circuit consists of threshold gates.
- The input is the primary opcode.
- It generates three types of controls, namely, instruction controls, register controls and Read/Write controls.

Arithmetic Logic Unit

- The ALU performs both arithmetic and logical operations.
- The data input is read from the register file, and the control input is given by the instruction decoder.
- The output is given to the register file and is stored in the register designated by the primary opcode.

Register File

- The Register file consists of four general-purpose registers and one temporary register .
- The temporary register supports the MOVE operation and is a simple ring structure.
- Register controls and the Read/Write controls are obtained from the instruction decoder.

Conclusion

- The operating principle and experimental results of a VGA circuit are described. Maintaining a constant inversion coefficient provided a reasonable tradeoff to maintain gain versus temperature. Measurement results satisfy the main specifications.
- The simulation data from the pipelined digital test circuits so far indicates that there might be an advantage to asynchronous logic (specifically delay-insensitive style) for low temperature and low power applications.
- To further research the characteristics of asynchronous logic under these conditions, an Asynchronous microcontroller is being designed that will be able to operate at cryogenic temperatures.